```
Your SELECT statement
   s gate and (alumina or aluminum(w)oxide or aluminate or sapphire) and
(silicon(w)monoxide or SiO) and (sputter? or evaporat? or cosputter? or
coevaporat?)

          Items   File
          -----   ----
              7     2: INSPEC_1969-2002/Feb W3
              1     6: NTIS_1964-2002/Mar W1
              2     8: Ei Compendex(R)_1970-2002/Feb W3
              1    35: Dissertation Abs Online_1861-2002/Feb
              1    95: TEME-Technology & Management_1989-2002Jan W3
      Examined  50 files
              3   340: CLAIMS(R)/US Patent_1950-02/Feb 19
              8   347: JAPIO_Oct/1976-2001/Oct(Updated 020204)
            195   348: EUROPEAN PATENTS_1978-2002/Feb W02
             59   349: PCT FULLTEXT_1983-2002/UB=20020214,UT=20020207

### Status: Break Sent.

?b 2,8,35,340
       21feb02 20:27:38 User264704 Session D99.4
            $3.96    2.265 DialUnits File411
     $3.96  Estimated cost File411
     $0.26  TYMNET
     $4.22  Estimated cost this search
    $21.99  Estimated total session cost   4.306 DialUnits


SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Feb W3
         (c) 2002 Institution of Electrical Engineers
  File   8:Ei Compendex(R)  1970-2002/Feb W3
         (c) 2002 Engineering Info. Inc.
  File  35:Dissertation Abs Online  1861-2002/Feb
         (c) 2002 ProQuest Info&Learning
  File 340:CLAIMS(R)/US Patent  1950-02/Feb 19
         (c) 2002 IFI/CLAIMS(R)
*File 340: has been reloaded.  Published applications are available.
See HELP NEWS 340 for details.

      Set  Items  Description
      ---  -----  -----------
?s gate and (alumina or aluminum(w)oxide or aluminate or sapphire) and (silicon(w)monox
ide or SiO) and (sputter? or evaporat? or cosputter? or coevaporat?)
          228422  GATE
           98357  ALUMINA
          289892  ALUMINUM
          491883  OXIDE
           18266  ALUMINUM(W)OXIDE
            8292  ALUMINATE
           26447  SAPPHIRE
          556876  SILICON
           39302  MONOXIDE
            1192  SILICON(W)MONOXIDE
          116757  SIO
          114764  SPUTTER?
          138692  EVAPORAT?
             913  COSPUTTER?
            1647  COEVAPORAT?
      S1      13  GATE AND (ALUMINA OR ALUMINUM(W)OXIDE OR ALUMINATE OR
                  SAPPHIRE) AND (SILICON(W)MONOXIDE OR SIO) AND (SPUTTER?
                  OR EVAPORAT? OR COSPUTTER? OR COEVAPORAT?)
?rd
>>>Duplicate detection is not supported for File 340.

>>>Records from unsupported files will be retained in the RD set.
```

none relevant all Al_2O_3 alone as gate diel.

```
Your SELECT statement i
   s (doped or dopant)(2n)oxide? and gate and (si or silicon) and (aluminum
or alumina)

          Items   File
          -----   ----
              2     2: INSPEC_1969-2002/Feb W3
              1     6: NTIS_1964-2002/Mar W1
              4     8: Ei Compendex(R)_1970-2002/Feb W3
              1    34: SciSearch(R) Cited Ref Sci_1990-2002/Feb W4
              2   108: AEROSPACE DATABASE_1962-2001/DEC
       Examined  50 files

### Status: Break Sent.

?b 2,8,108;s (doped or dopant)(2n)oxide? and gate and (si or silicon) and (aluminum or
alumina)
       21feb02 20:18:02 User264704 Session D99.2
            $2.15    1.226 DialUnits File411
     $2.15  Estimated cost File411
     $0.26  TYMNET
     $2.41  Estimated cost this search
     $2.42  Estimated total session cost   1.462 DialUnits


SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Feb W3
         (c) 2002 Institution of Electrical Engineers
  File   8:Ei Compendex(R)  1970-2002/Feb W3
         (c) 2002 Engineering Info. Inc.
  File 108:AEROSPACE DATABASE  1962-2001/DEC
         (c) 2002 AIAA
*File 108: For update information please see Help News108.

      Set  Items  Description
      ---  -----  -----------
          177732  DOPED
           27428  DOPANT
          378377  OXIDE?
            4820  (DOPED OR DOPANT)(2N)OXIDE?
          122366  GATE
          378434  SI
          497090  SILICON
          249132  ALUMINUM
           69149  ALUMINA
      S1       8  (DOPED OR DOPANT)(2N)OXIDE? AND GATE AND (SI OR SILICON)
                  AND (ALUMINUM OR ALUMINA)
?rd
...completed examining records
      S2       5  RD (unique items)
?t s2/full/all
```

2/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6874409 INSPEC Abstract Number: B2001-04-2570D-029

Title: Si **-doped aluminates for high temperature metal-** gate **CMOS: Zr-Al-** Si **-O, a novel** gate **dielectric for low power applications**

Author(s): Manchanda, L.; Green, M.L.; van Dover, R.B.; Morris, M.D.; Kerber, A.; Hu, Y.; Han, J.-P.; Silverman, P.J.; Sorsch, T.W.; Weber, G.; Donnelly, V.; Pelhos, K.; Klemens, F.; Ciampa, N.A.; Kornblit, A.; Kim, Y.O.; Bower, J.E.; Barr, D.; Ferry, E.; Jacobson, D.; Eng, J.; Busch, B.; Schulte, H.

Author Affiliation: Lucent Technol. Bell Labs., Murray Hill, NJ, USA

Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.23-6

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA 871 pp.

ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191

U.S. Copyright Clearance Center Code: 0 7803 6438 4/2000/$10.00

Conference Title: International Electron Devices Meeting. Technical Digest. IEDM

Conference Sponsor: Electron Devices Soc. IEEE

Conference Date: 10-13 Dec. 2000 Conference Location: San Francisco, CA, USA

Medium: Also available on CD-ROM in PDF format

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P); Experimental (X)

Abstract: We have investigated a new class of high K **gate** dielectric materials, **Si** -doped aluminates. These dielectrics, with TiN gates, can withstand high temperature CMOS processing and therefore do not require replacement **gate** technology. In this paper we focus on **Si** -doped zirconium aluminate (Zr-Al- **Si** -O), with K~20. With the TiN **gate** stack subjected to the standard CMOS thermal budget, we have scaled this dielectric to t/sub eq/~1.2 nm with leakage current <50 mA/cm/sup 2/ and **gate** power budget <50 mW/cm/sup 2/, at IV. For high performance, low power CMOS, beyond SiO/sub 2/, **doped - aluminum oxide** (with K~10) may be a viable alternate **gate** dielectric. Beyond **aluminum** oxide, aluminates (with K>15) may be viable alternate **gate** dielectrics. (7 Refs)

Subfile: B

Descriptors: CMOS integrated circuits; dielectric thin films; leakage currents; low-power electronics; zirconium compounds

Identifiers: high temperature metal- **gate** CMOS; **gate** dielectric; low power applications; **gate** stack; leakage current; **gate** power budget; 1 V ; 1.2 nm; ZrAlSiO

Class Codes: B2570D (CMOS integrated circuits); B2810 (Dielectric materials and properties)

Chemical Indexing:

ZrAlSiO int - Al int - Si int - Zr int - O int - ZrAlSiO ss - Al ss - Si ss - Zr ss - O ss (Elements - 4)

Numerical Indexing: voltage 1.0E+00 V; size 1.2E-09 m

2/9/2 (Item 2 from [redacted]e: 2)
DIALOG(R)File 2:INSPEC

01558362 INSPEC Abstract Number: B80039984
Title: A silicon **and** aluminum **dynamic memory technology**
Author(s): Larsen, R.A.
Author Affiliation: IBM General Technol. Div. Lab., Essex Junction, VT, USA
Journal: IBM Journal of Research and Development vol.24, no.3 p. 268-82
Publication Date: May 1980 Country of Publication: USA
CODEN: IBMJAE ISSN: 0018-8646
Language: English Document Type: Journal Paper (JP)
Treatment: General, Review (G); Experimental (X)
Abstract: The **Silicon** and **Aluminum** Metal Oxide Semiconductor (SAMOS) technology is presented as a high-yield, low-cost process to make one-device-cell random access memories. The characteristics of the process are a multilayer dielectric **gate** insulator (oxide-nitride), a p-type polysilicon field shield, and a **doped oxide** diffusion source. Added yield-enhancing features are backside ion implant gettering, dual dielectric insulators between metal layers, and circuit redundancy. A family of chips is produced using SAMOS, ranging from 18K bits to 64K bits. System features such as on-chip data registers are designed on some chips. The chip technology is merged with 'flip-chip' packaging to provide one-inch-square modules from 72K bits through 512K bits, with typical access times from 90 ns to 300 ns. (49 Refs)
Subfile: B
Descriptors: field effect integrated circuits; integrated circuit technology; integrated memory circuits; large scale integration; random-access storage
Identifiers: SAMOS; multilayer dielectric **gate** insulator; **doped oxide** diffusion source; backside ion implant gettering; dual dielectric insulators between metal layers; circuit redundancy; dynamic RAM technology ; IBM; **Si** and Al MOS; one device per cell RAM; p-type poly- **Si** field shield; 18K to 64K RAM; flip chip packaging
Class Codes: B1265D (Memory circuits); B2570F (Other MOS integrated circuits)

2/9/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02354168 E.I. Monthly No: EIM8711-080403
Title: HYDROGEN DIFFUSION IN PLASMA DEPOSITED SILICON **NITRIDE-** ALUMINUM **INTERFACE UNDER PLASMA PROCESSING AND ITS EFFECT ON FET DEVICE V//T SHIFT.**
Author: Nguyen, S. V.; Kim, S. U.
Corporate Source: IBM, Essex Junction, VT, USA
Conference Title: Extended Abstracts - Fall Meeting (168th Society Meeting), the Electrochemical Society.
Conference Location: Las Vegas, NV, USA Conference Date: 19851013
Sponsor: Electrochemical Soc, Pennington, NJ, USA
E.I. Conference No.: 09038
Source: Electrochemical Society Extended Abstracts v 85-2. Publ by Electrochemical Soc, Pennington, NJ, USA p 437-438
Publication Year: 1985
CODEN: ESABB6 ISSN: 0160-4619
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8711
Abstract: The presence of hydrogen in thin **silicon** nitride films has a dramatic effect on the physical, chemical, and electrical properties of the films. During microelectronic circuit fabrication, processing cycles such as dopant drive-in, annealing, and plasma etching in the presence of high hydrogen content plasma **silicon** nitride layers may cause hydrogen bonding rearrangement and hydrogen atom diffusion, and thus generate adverse effects on the films and device properties. In a recent study, negative V//T shift encountered in the RIE etching of passivated plasma **silicon** nitride layers were found to be dependent on etching process condition and the **gate** oxide thickness. However, the qualitative of V//T shift is also found to be strongly dependent on the deposited **silicon** nitride films. In an effort to understand this dependency, we have investigated the hydrogen bonding and diffusion between the plasma deposited and after-plasma RIE (reactive ion etching) using the Fourier transformed infrared (FTIR) and Nuclear Reaction Analysis techniques. **Silicon** nitride films were deposited on 100 mm bare **silicon** , p-type wafers. (Edited author abstract) 8 refs.
Descriptors: SEMICONDUCTING **SILICON** --*Coatings; **SILICON** NITRIDE--Thin Films; HYDROGEN--Diffusion; MICROELECTRONICS--Materials
Identifiers: **GATE OXIDE** ; **DOPANT** DRIVE-IN; HYDROGEN BONDING; P-TYPE WAFERS; EXTENDED ABSTRACT
Classification Codes:
712 (Electronic & Thermionic Materials); 813 (Coatings & Finishes); 812 (Ceramics & Refractories); 714 (Electronic Components); 804 (Chemical Products); 931 (Applied Physics)
71 (ELECTRONICS & COMMUNICATIONS); 81 (CHEMICAL PROCESS INDUSTRIES); 80 (CHEMICAL ENGINEERING); 93 (ENGINEERING PHYSICS)

2/9/4 (Item 2 from [redacted]: 8)
DIALOG(R)File 8:Ei Compendex(R)

00741662 E.I. Monthly No: EI7809069256 E.I. Yearly No: EI78075694
Title: C-MOS Processes for Integrated Circuits.
Title: HALBLEITERPROZESSE FUER KOMPLEMENTAERSCHALTUNGEN.
Author: Splittgerber, Heinz
Corporate Source: Siemens, Munich, Ger
Source: Bundesministerium fuer Forschung und Technologie, Forschungsbericht, Technologische Forschung und Entwicklung n T 77-30 Dec 1977 50 p
Publication Year: 1977
CODEN: BFTEAJ ISSN: 0340-7608
Language: GERMAN
Journal Announcement: 7809
Abstract: Various complementary ESFI-SOS processes are described. First, a simple process is shown in the **aluminum - gate** technology. Furthermore the process with selective doping and the so-called ESFION process (selfalignment by ion implantation) are given. A self-aligned **silicon gate** process is explained. The laser scribing for dividing the sapphire substrates, the use of undoped and **doped** pyrolytic **oxides** is described. 33 refs. In German with English abstract.
Descriptors: *SEMICONDUCTOR DEVICE MANUFACTURE
Classification Codes:
714 (Electronic Components)
71 (ELECTRONICS & COMMUNICATIONS)

2/9/5 (Item 1 from [redacted]e: 108)
DIALOG(R)File 108:AEROSPACE DATABASE

00745605 N75-11782
Investigation of chromium- doped oxides
Final Report, 1 Nov. 1971 - 1 Nov. 1973
KJAR, R. A.
Rockwell International Corp., Anaheim, CA. Electronics Research Div.
CORPORATE CODE: RY230143
Nov. 1973 155P.
REPORT NO.: AD-783988; C71-1063/501
CONTRACT NO.: N00014-72-C-0017
LANGUAGE: English
COUNTRY OF ORIGIN: United States COUNTRY OF PUBLICATION: United States
DOCUMENT TYPE: REPORT
DOCUMENTS AVAILABLE FROM AIAA Technical Library
OTHER AVAILABILITY: NTIS
JOURNAL ANNOUNCEMENT: STAR7502

Part I of the report describes results obtained during the investigation of the mechanisms by which chromium-doping of a **silicon** -dioxide **gate** insulator may improve the radiation resistance of MOS devices. Part II details the fabrication and testing of a CMOS/SOS 4-bit adder that employed chrome-doped and **aluminum** ion-implanted **gate** oxides to provide improved radiation hardness. (DTIC)

SOURCE OF ABSTRACT/SUBFILE: DTIC
DESCRIPTORS: *ADDING CIRCUITS; *INTEGRATED CIRCUITS; *METAL OXIDE SEMICONDUCTORS; *RADIATION HARDENING; CHROMIUM ISOTOPES; ELECTRICAL PROPERTIES; MATERIALS TESTS; SAPPHIRE; **SILICON** COMPOUNDS
SUBJECT CLASSIFICATION: 7576 Solid-State Physics (1975-)
COSATI CODE: 20L Solid-state Physics